FIG. 1

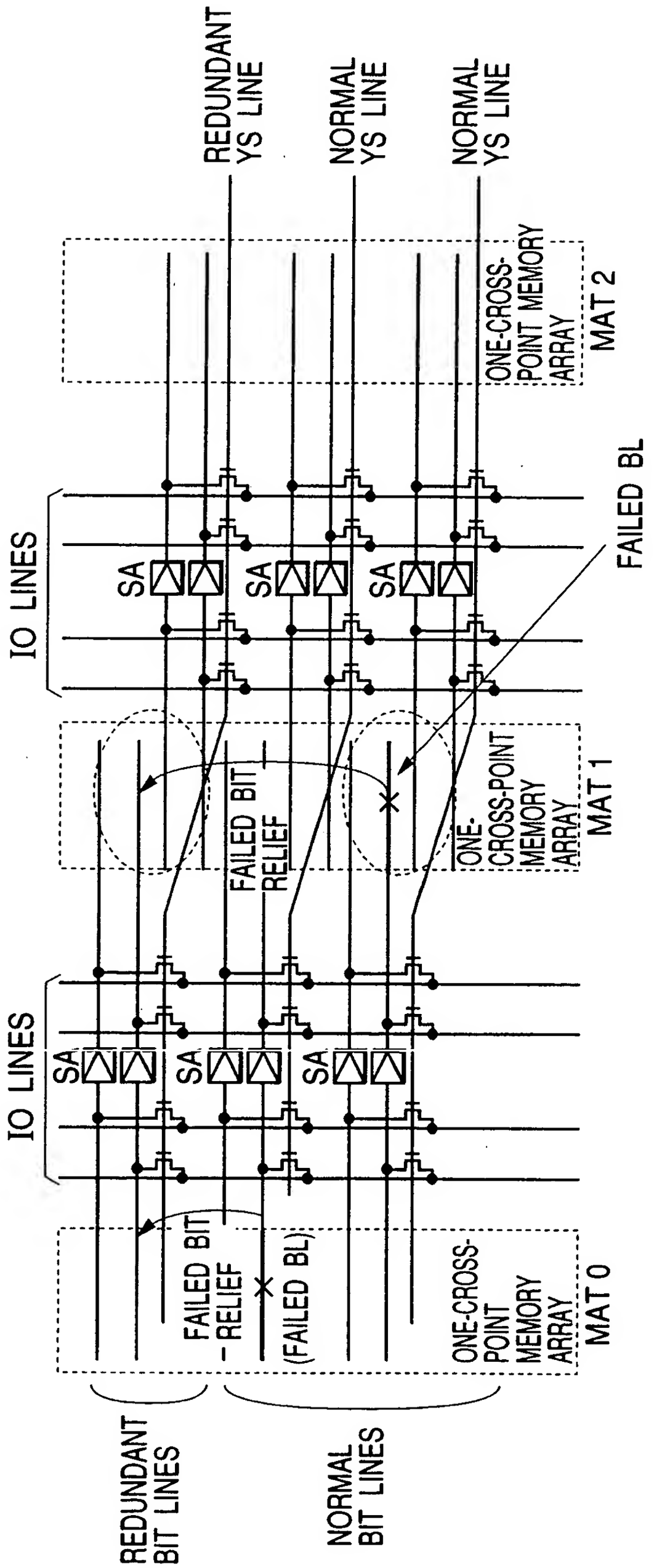

REDUNDANT YS LINE
NORMAL YS LINE
NORMAL YS LINE
ONE-CROSS-POINT MEMORY ARRAY
MAT 2
IO LINES
SA
SA
SA
FAILED BL
FAILED BIT RELIEF
ONE-CROSS-POINT MEMORY ARRAY
MAT 1
IO LINES
SA
SA
SA
FAILED BIT RELIEF
(FAILED BL)
ONE-CROSS-POINT MEMORY ARRAY
MAT 0
REDUNDANT BIT LINES
NORMAL BIT LINES

FIG. 2

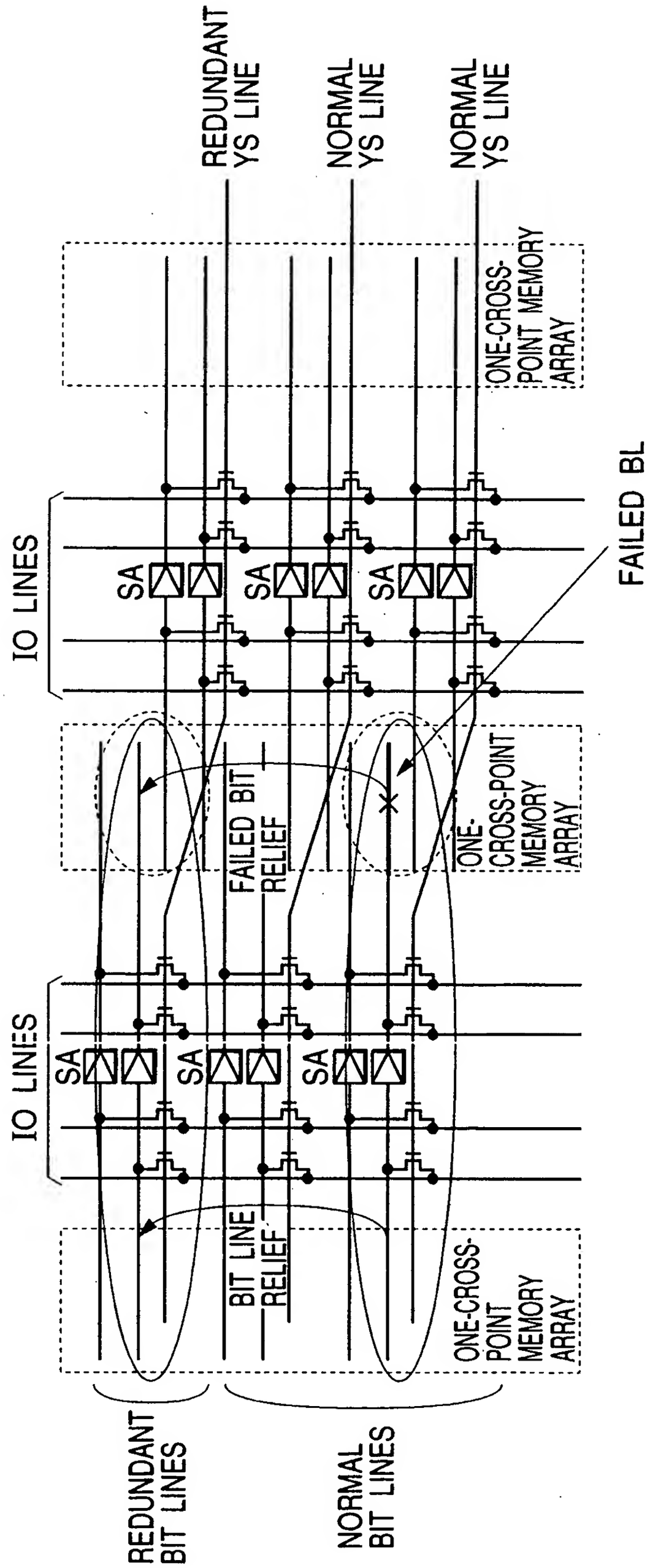

REDUNDANT YS LINE
NORMAL YS LINE
NORMAL YS LINE
ONE-CROSS-POINT MEMORY ARRAY
IO LINES
SA
SA
SA
FAILED BIT RELIEF
FAILED BL
ONE-CROSS-POINT MEMORY ARRAY
IO LINES
SA
SA
SA
BIT LINE RELIEF
ONE-CROSS-POINT MEMORY ARRAY
REDUNDANT BIT LINES
NORMAL BIT LINES

FIG. 3

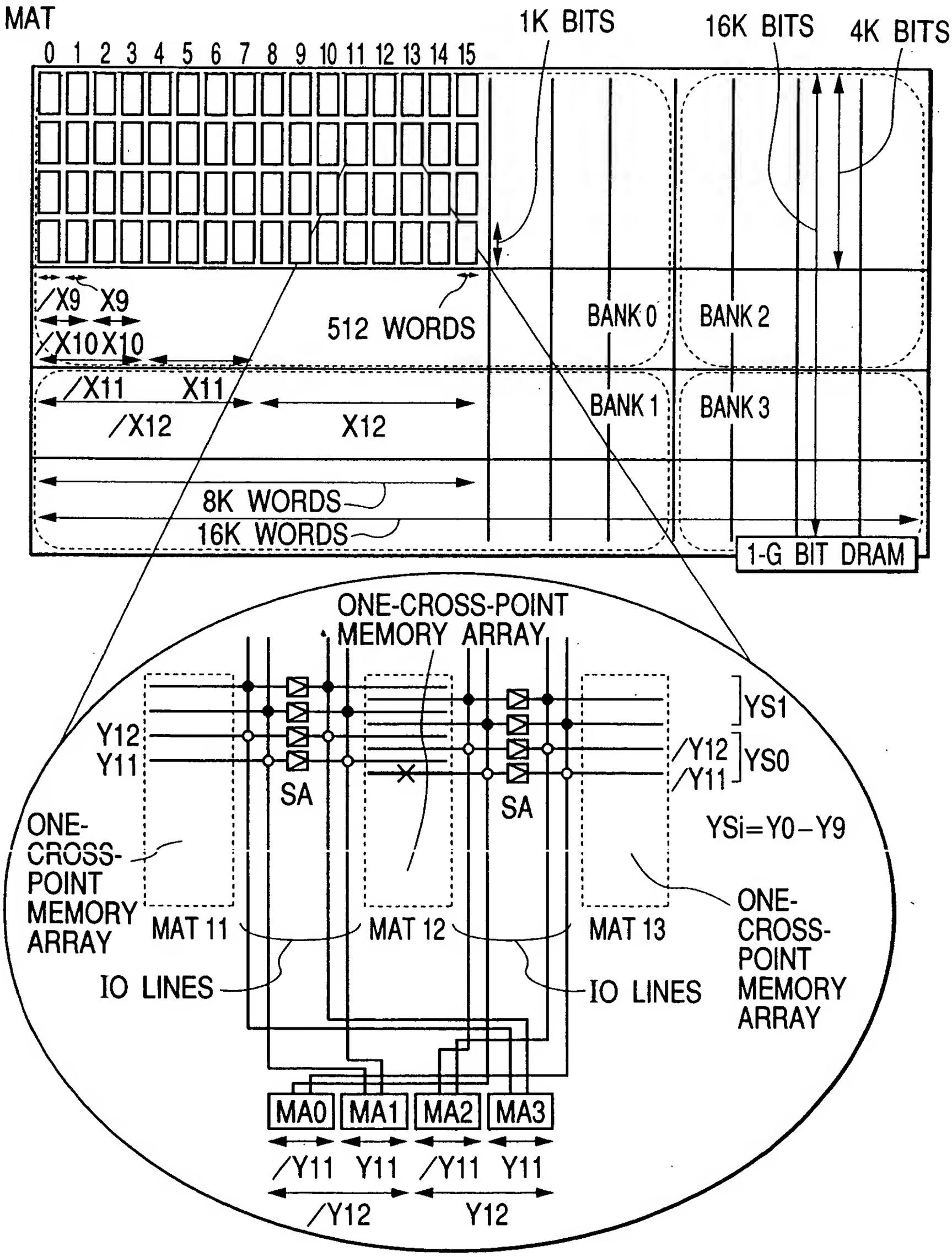
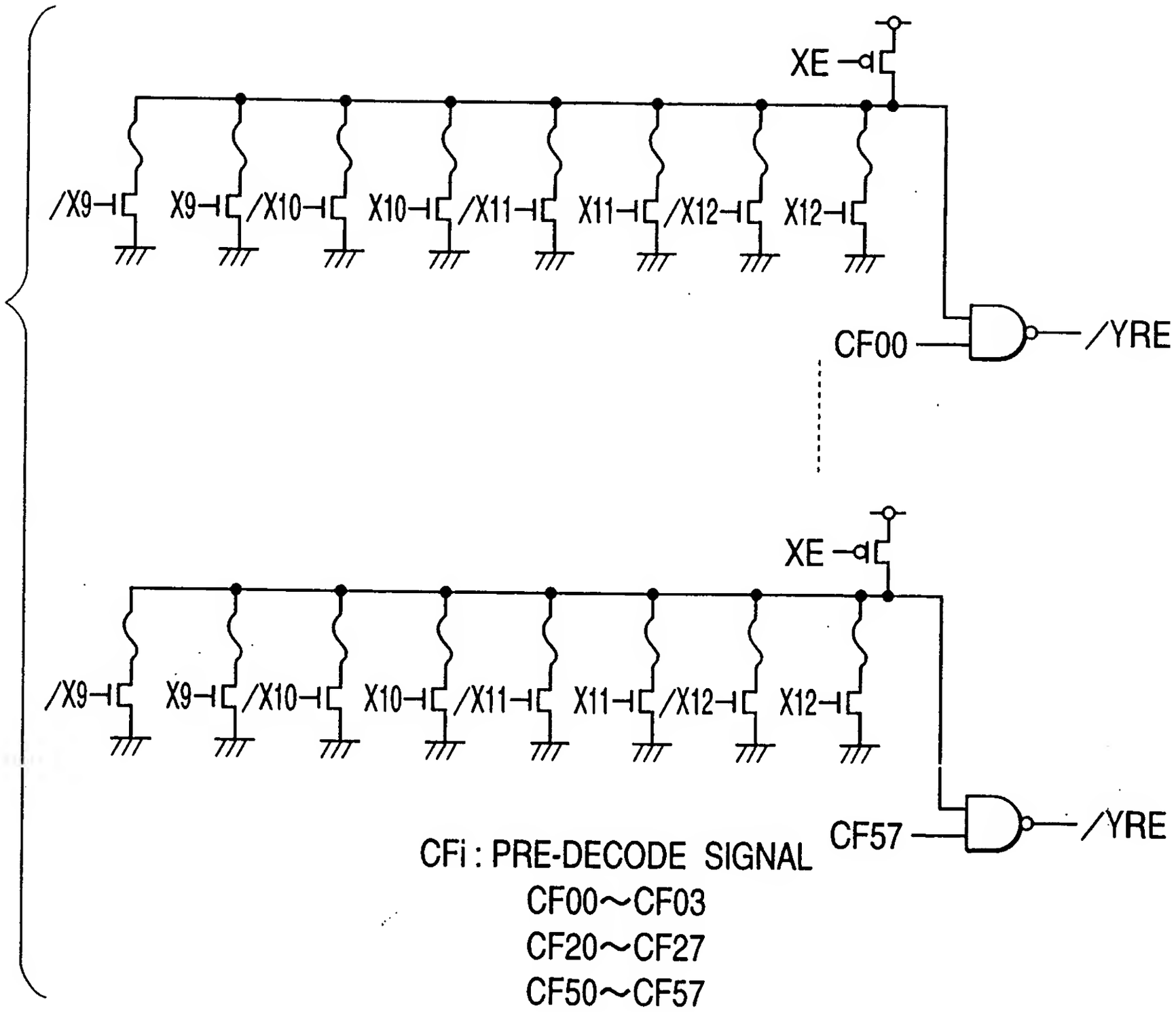
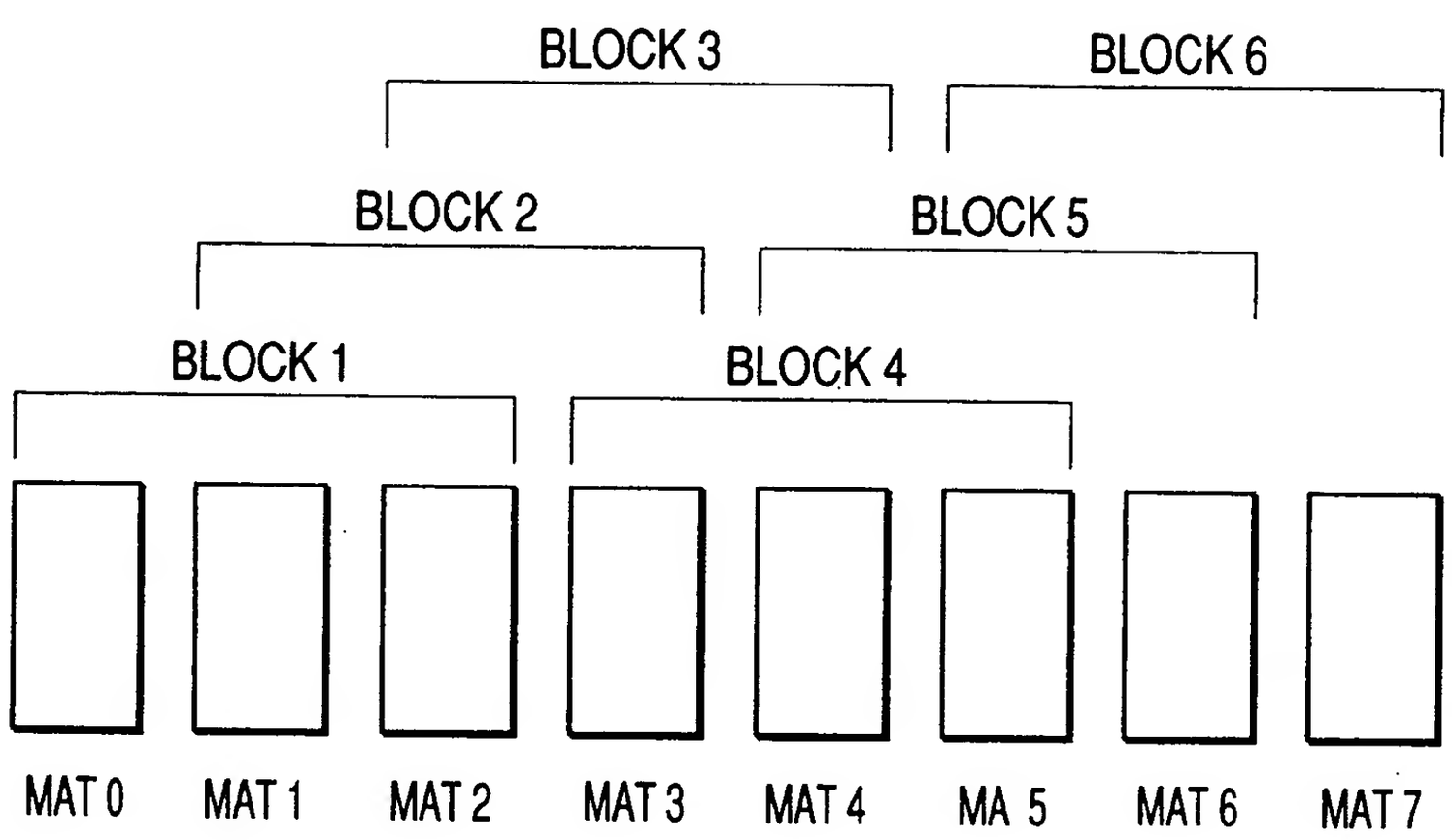

MAT
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
1K BITS
16K BITS
4K BITS
/X9
X9
/X10
X10
512 WORDS
BANK 0
BANK 2
/X11
X11
/X12
X12
BANK 1
BANK 3
8K WORDS
16K WORDS
1-G BIT DRAM
ONE-CROSS-POINT MEMORY ARRAY
Y12
Y11
SA
SA
YS1
/Y12
/Y11
YS0
YSi=Y0−Y9
ONE-CROSS-POINT MEMORY ARRAY
MAT 11
MAT 12
MAT 13
IO LINES
IO LINES
ONE-CROSS-POINT MEMORY ARRAY
MA0
MA1
MA2
MA3
/Y11
Y11
/Y11
Y11
/Y12
Y12

FIG. 4



CFi : PRE-DECODE SIGNAL
CF00~CF03
CF20~CF27
CF50~CF57

FIG. 5



WHEN FAILED BIT LINE ON MAT 0 OR 1 ···· BLOCK 1 RELIEVED
WHEN FAILED BIT LINE ON MAT 2 ····· BLOCK 2 RELIEVED
WHEN FAILED BIT LINE ON MAT 3 ····· BLOCK 3 RELIEVED
WHEN FAILED BIT LINE ON MAT 4 ····· BLOCK 4 RELIEVED
WHEN FAILED BIT LINE ON MAT 5 ····· BLOCK 5 RELIEVED
WHEN FAILED BIT LINE ON MAT 6 OR 7 ···· BLOCK 6 RELIEVED

FIG. 6

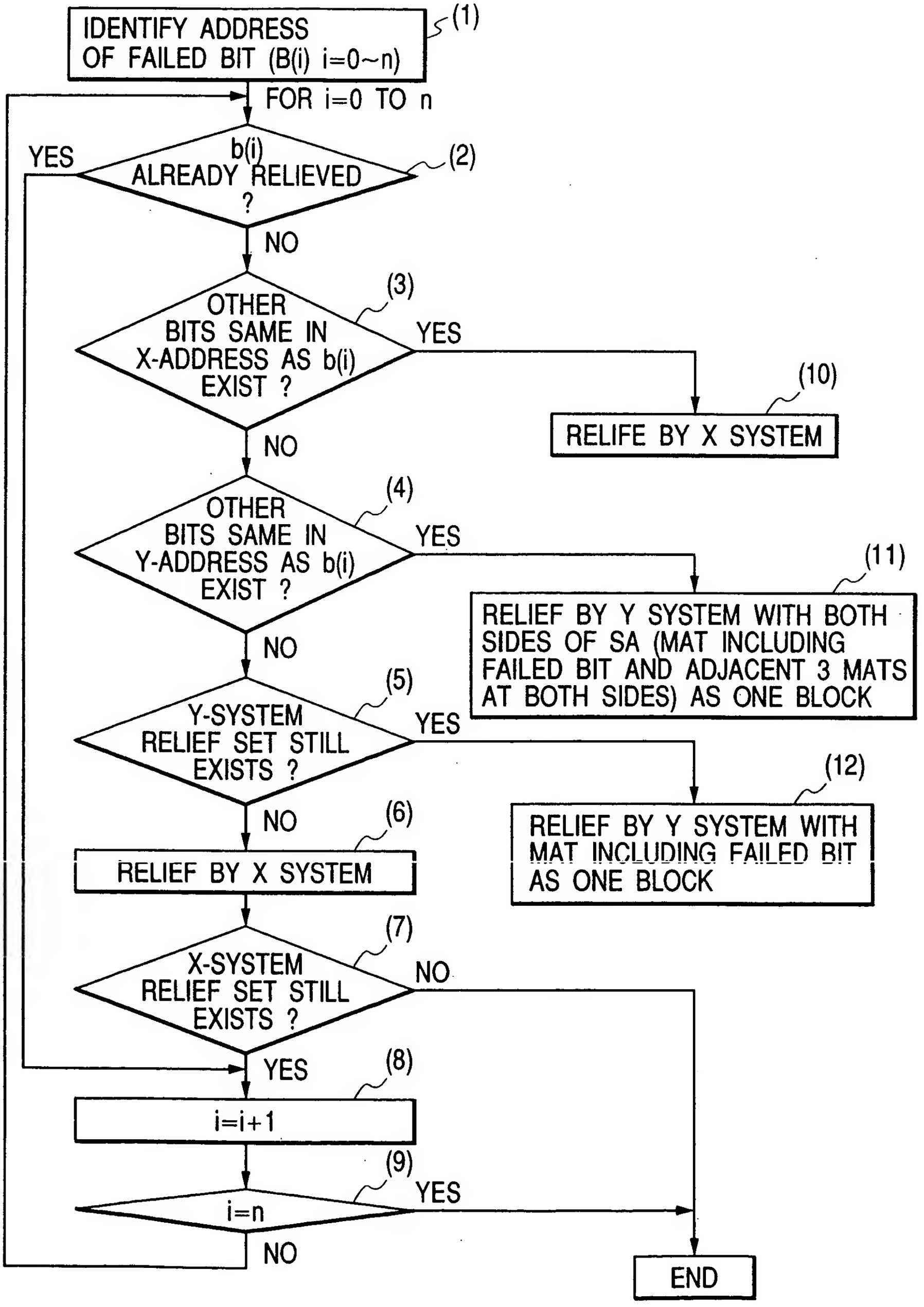

IDENTIFY ADDRESS OF FAILED BIT (B(i) i=0~n)
(1)
FOR i=0 TO n
b(i) ALREADY RELIEVED ?
(2)
YES
NO
OTHER BITS SAME IN X-ADDRESS AS b(i) EXIST ?
(3)
YES
(10)
RELIFE BY X SYSTEM
NO
OTHER BITS SAME IN Y-ADDRESS AS b(i) EXIST ?
(4)
YES
(11)
RELIEF BY Y SYSTEM WITH BOTH SIDES OF SA (MAT INCLUDING FAILED BIT AND ADJACENT 3 MATS AT BOTH SIDES) AS ONE BLOCK
NO
Y-SYSTEM RELIEF SET STILL EXISTS ?
(5)
YES
(12)
RELIEF BY Y SYSTEM WITH MAT INCLUDING FAILED BIT AS ONE BLOCK
NO
(6)
RELIEF BY X SYSTEM
X-SYSTEM RELIEF SET STILL EXISTS ?
(7)
NO
YES
(8)
i=i+1
(9)
i=n
YES
NO
END

FIG. 7

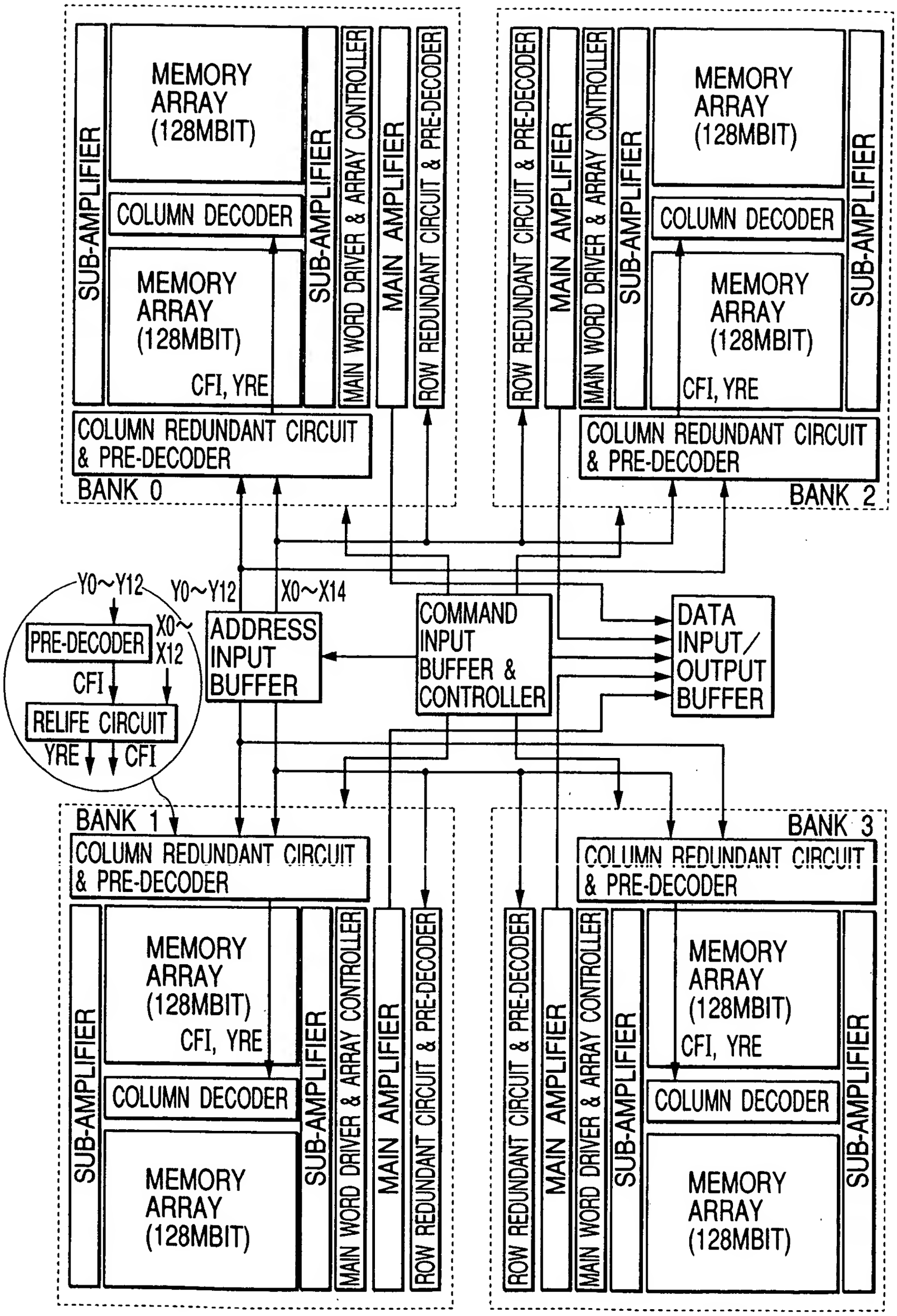

BANK 0
BANK 1
BANK 2
BANK 3
MEMORY ARRAY (128MBIT)
CFI, YRE
COLUMN DECODER
SUB-AMPLIFIER
MAIN WORD DRIVER & ARRAY CONTROLLER
MAIN AMPLIFIER
ROW REDUNDANT CIRCUIT & PRE-DECODER
COLUMN REDUNDANT CIRCUIT & PRE-DECODER
Y0~Y12
X0~X14
X0~X12
PRE-DECODER
CFI
RELIFE CIRCUIT
YRE
ADDRESS INPUT BUFFER
COMMAND INPUT BUFFER & CONTROLLER
DATA INPUT/ OUTPUT BUFFER

FIG. 8

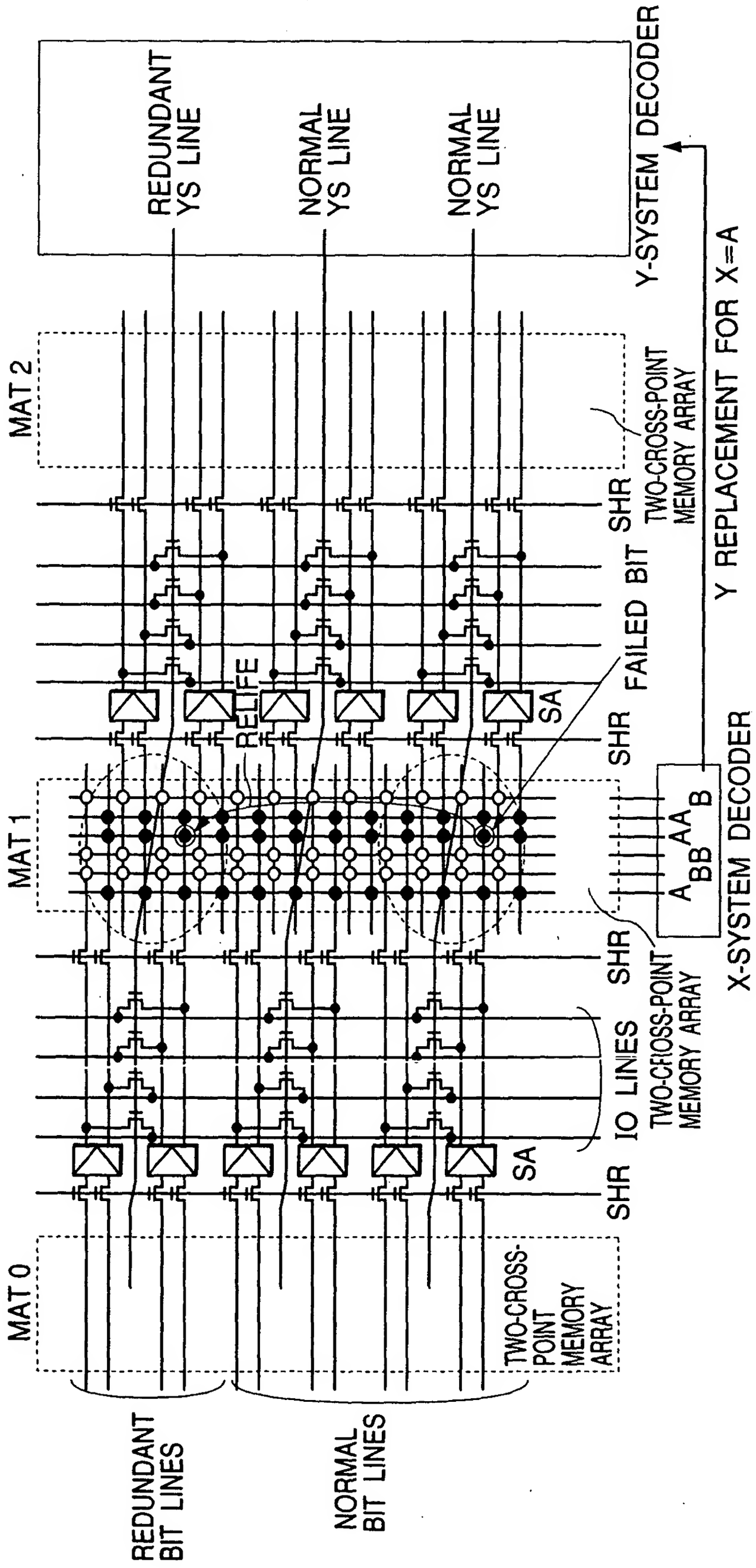

REDUNDANT YS LINE
NORMAL YS LINE
NORMAL YS LINE
Y-SYSTEM DECODER
Y REPLACEMENT FOR X=A
MAT 2
RELIFE
SA
SHR
FAILED BIT
SHR
TWO-CROSS-POINT MEMORY ARRAY
MAT 1
SHR
IO LINES
TWO-CROSS-POINT MEMORY ARRAY
X-SYSTEM DECODER
A
BB
AA
B
SA
SHR
MAT 0
TWO-CROSS-POINT MEMORY ARRAY
REDUNDANT BIT LINES
NORMAL BIT LINES

FIG. 9

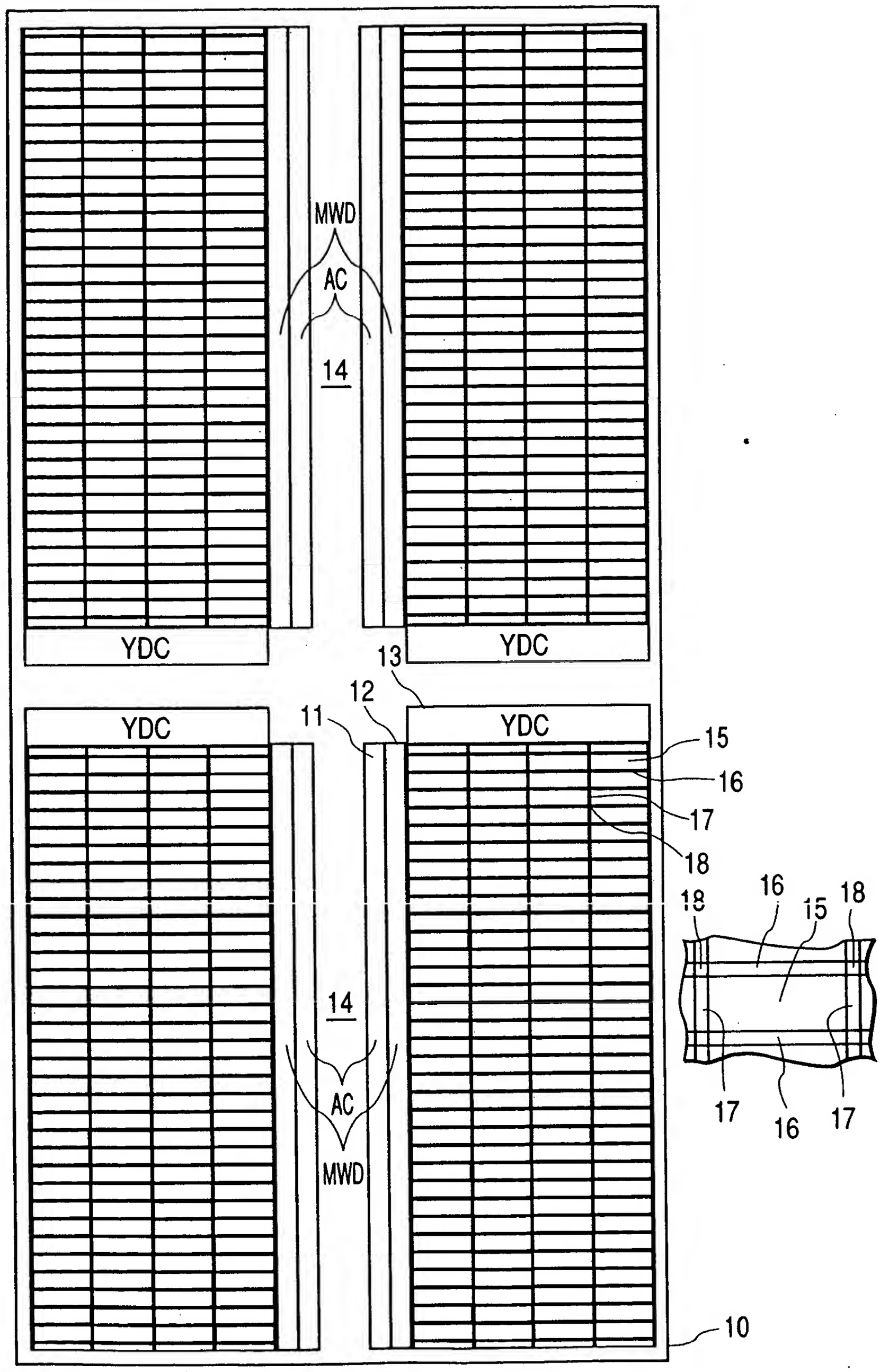

MWD
AC
14
YDC
YDC
13
12
11
YDC
YDC
15
16
17
18
14
AC
MWD
10
16
18
15
17
16
17

FIG. 10(a)

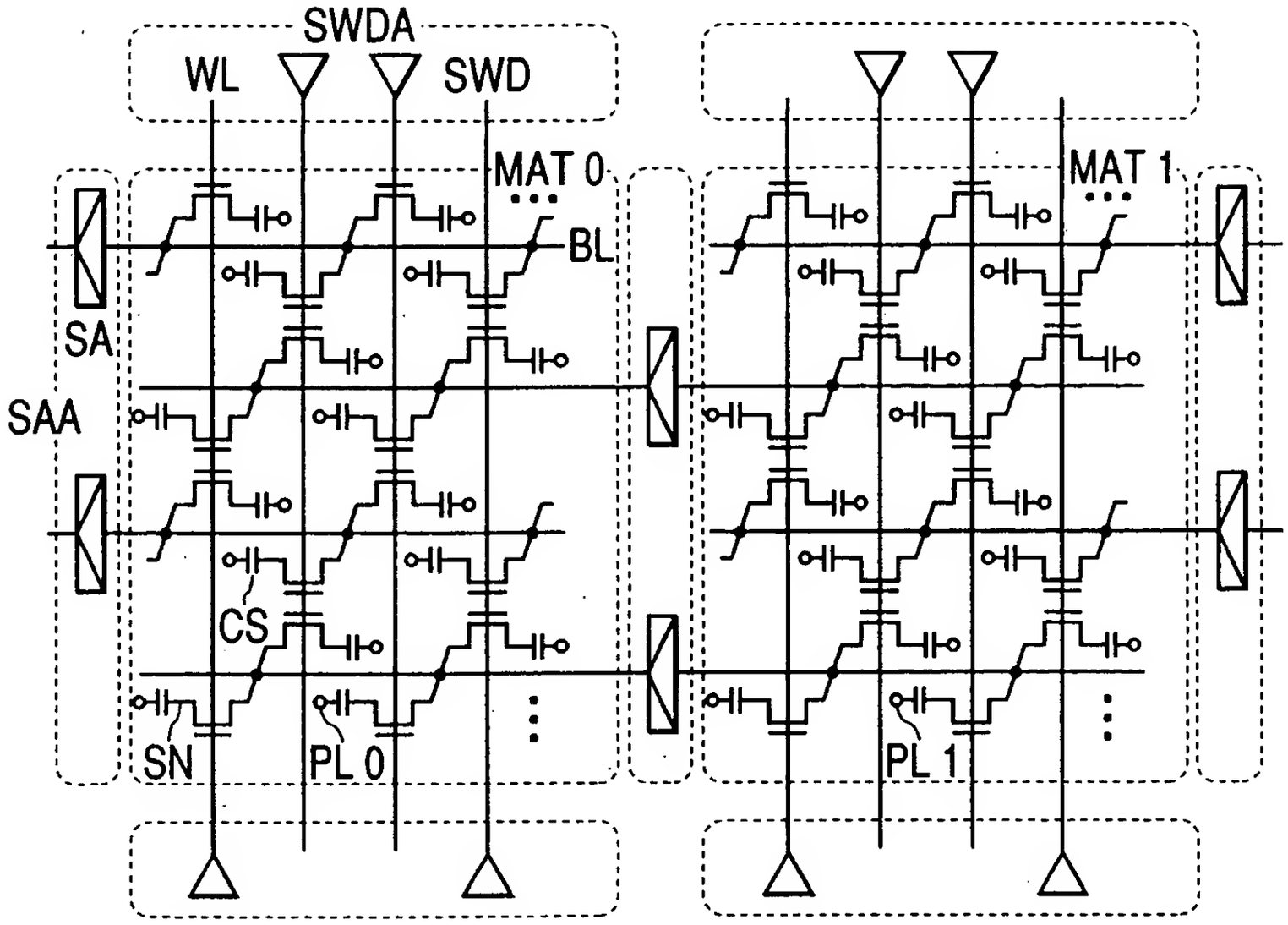


FIG. 10(b)

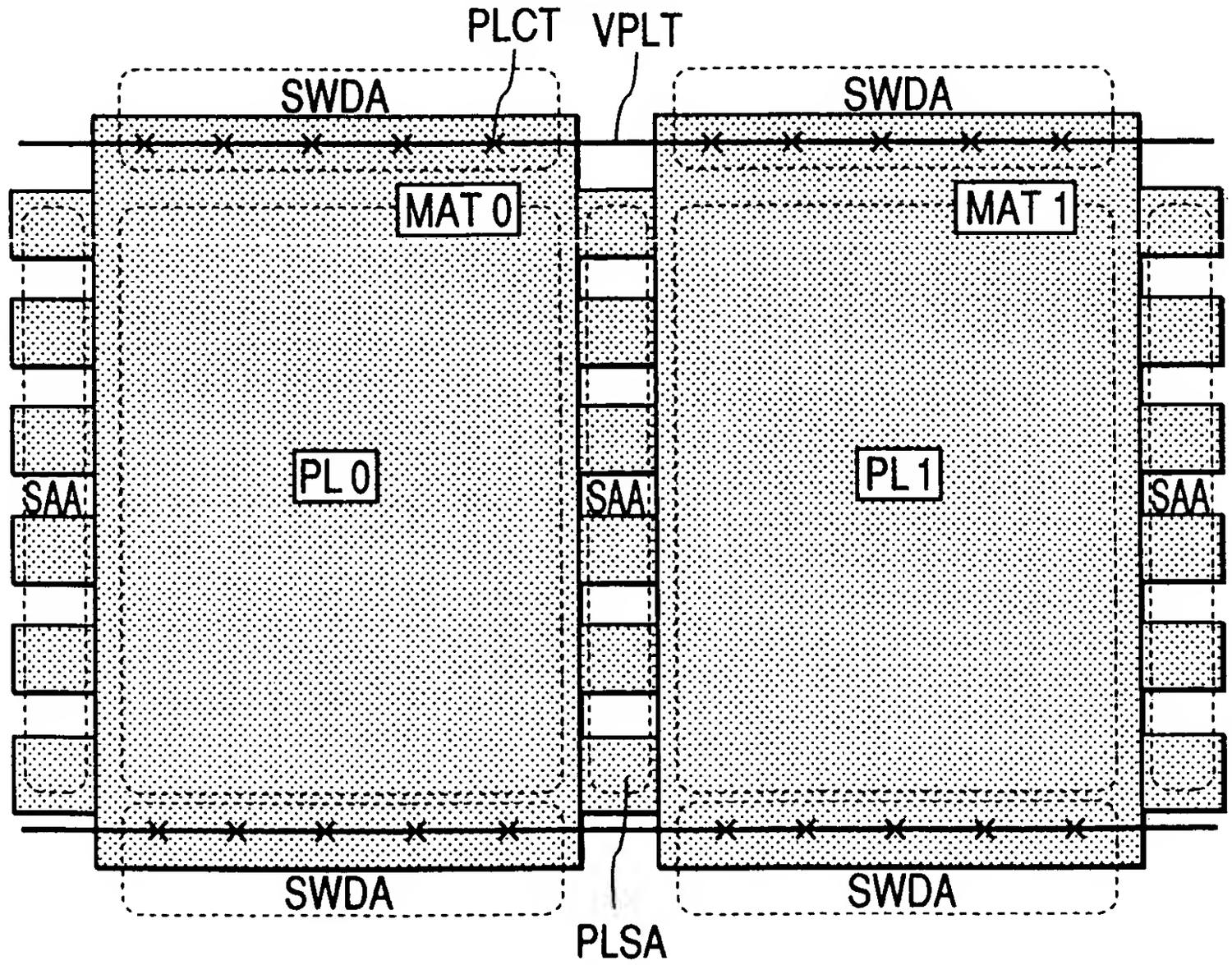


FIG. 11(a)

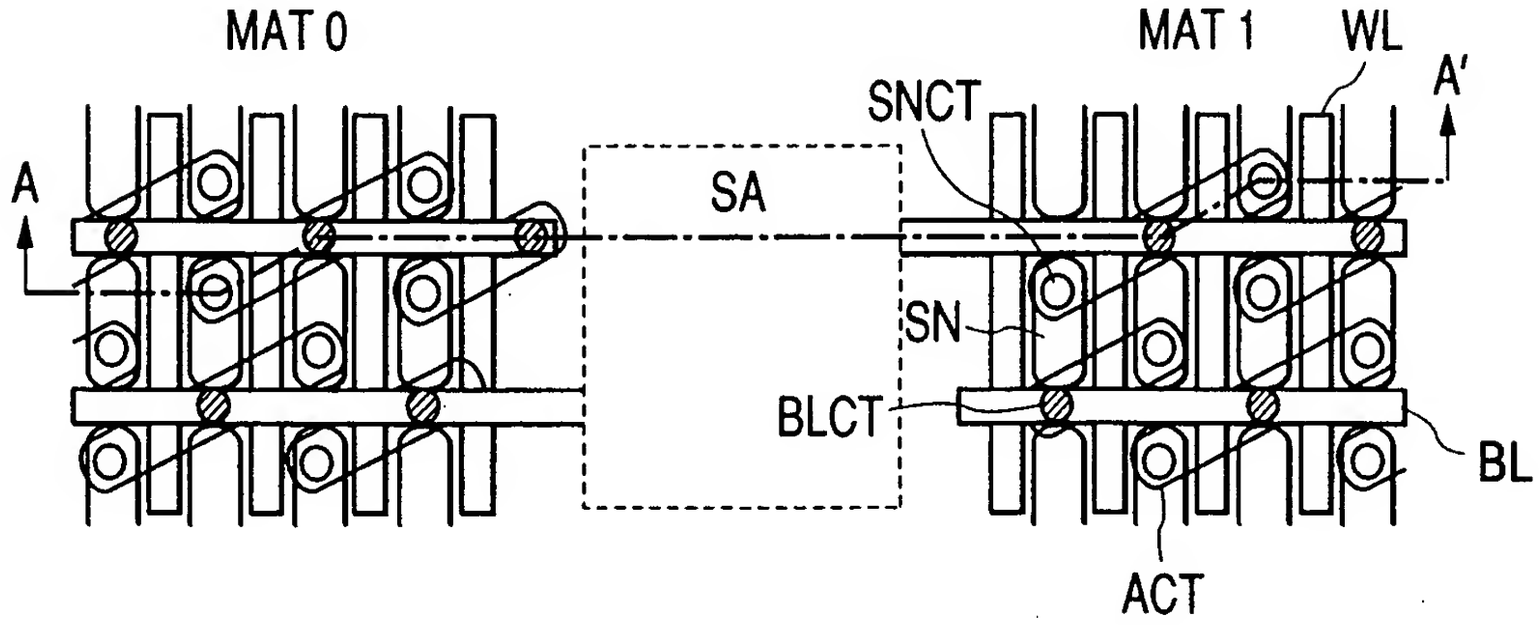
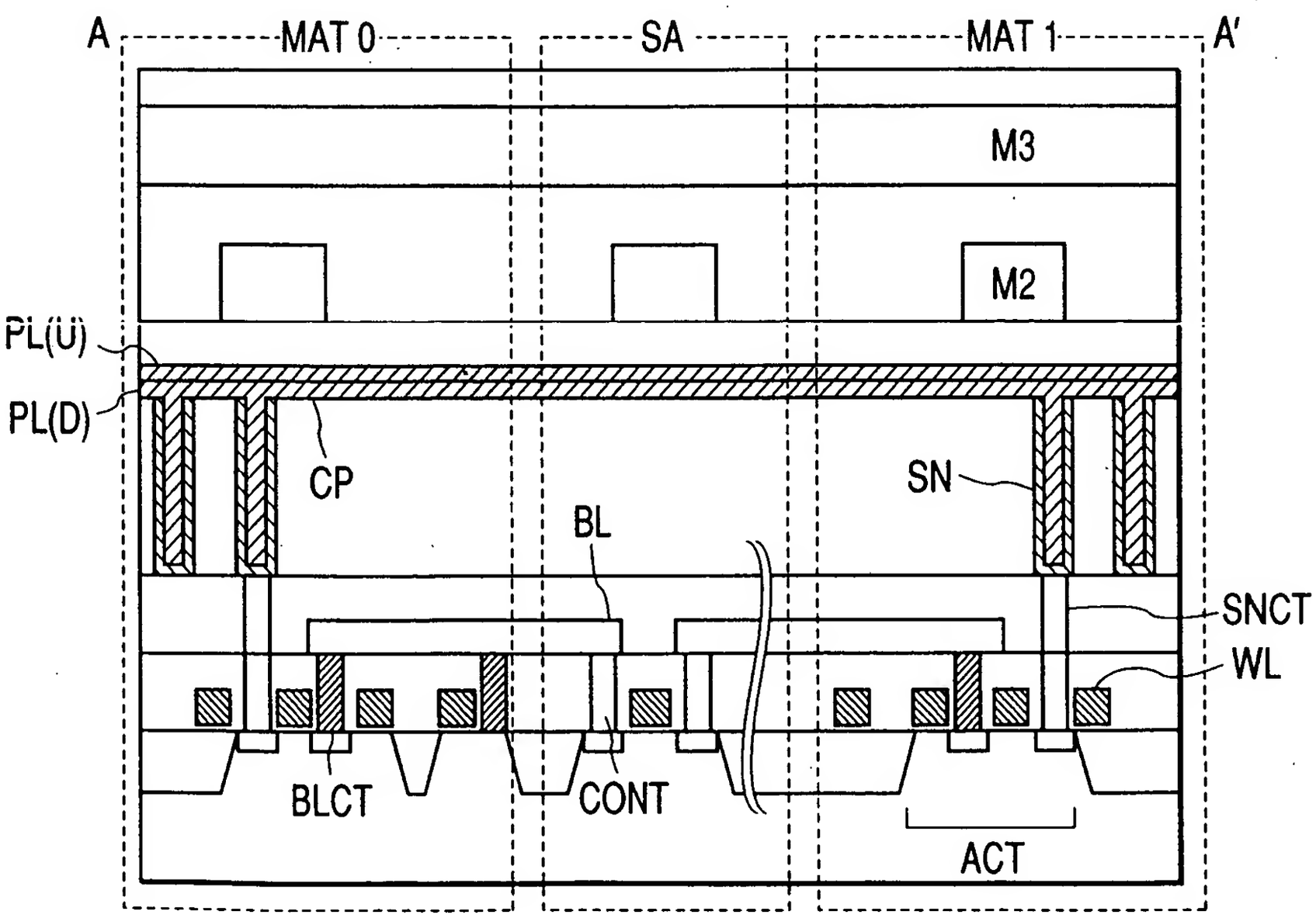



FIG. 11(b)